AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A clock data recovery circuit comprising:

a voltage control oscillator that generates a clock;

a data identifier that identifies input data based on [[a]] the clock generated by [[a]] the voltage control oscillator;

a frequency divider that divides a frequency of the input data; and

a phase comparator that detects a phase difference between a phase of the clock generated by the voltage control oscillator and a phase of the input data of which frequency is divided by the frequency divider, and generates a phase difference signal to eliminate the detected phase difference~~; and~~,

wherein the voltage control oscillator ~~that~~ generates the clock by adjusting an oscillation frequency based on the phase difference signal, and outputs the clock to both the data identifier and the phase comparator.

2. (Original) The clock data recovery circuit according to claim 1, further comprising:

a variable delaying unit that generates a delay clock which is obtained by delaying the clock generated by the voltage control oscillator by a predetermined time, between the voltage control oscillator and the phase comparator,

wherein the phase comparator detects a phase difference between a phase of the delay clock and a phase of input data of which frequency is divided by the frequency divider, and generates the phase difference signal.

3. (Currently Amended) The clock data recovery circuit according to claim 2, wherein the predetermined time to be used to delay the clock generated by the voltage control oscillator is set ~~at the~~ outside the voltage control oscillator.

4. (Original) The clock data recovery circuit according to claim 2, further comprising:

a duty ratio detector that determines a delay time to be used to delay the clock generated by the voltage control oscillator based on a duty ratio of the input data, and outputs the determined delay time to the variable delaying unit.

5. (Withdrawn) The clock data recovery circuit according to claim 1, further comprising:

a variable delaying unit that generates a delayed frequency-divided input data which is obtained by delaying the input data of which frequency is divided by the frequency divider by a predetermined time, between the frequency divider and the phase comparator, wherein

the phase comparator detects a phase difference between a phase of the clock generated by the voltage control oscillator and a phase of the delayed frequency-divided input data, and generates the phase difference signal.

6. (Withdrawn) The clock data recovery circuit according to claim 5,

wherein the predetermined time to be used to delay the input data of which frequency is divided by the frequency divider is set at the outside.

7. (Withdrawn) The clock data recovery circuit according to claim 5, further comprising:

a duty ratio detector that determines a delay time to be used to delay the input data of which frequency is divided by the frequency divider based on a duty ratio of the input data, and outputs the determined delay time to the variable delaying unit.

8. (Withdrawn) The clock data recovery circuit according to claim 1, further comprising:

a variable delaying unit that generates delayed input data obtained by delaying the input data by a predetermined time, at a front stage of the data identifier,

wherein the data identifier identifies the delayed input data based on the clock generated by the voltage control oscillator.

9. (Withdrawn) The clock data recovery circuit according to claim 8,

wherein the predetermined time to be used to delay the input data is set at the outside.

10. (Withdrawn) The clock data recovery circuit according to claim 8, further comprising:

a duty ratio detector that determines a delay time to be used to delay the input data based on a duty ratio of the input data, and outputs the determined delay time to the variable delaying unit.

11. (Withdrawn) A clock data recovery circuit comprising:

a first clock generating circuit that generates a first clock synchronous with a rise of input data;

a second clock generating circuit that generates a second clock synchronous with a fall of the input data;

a phase combiner that combines the first clock with the second clock, and outputs a clock of an intermediate phase between a phase of the first clock and a phase of the second clock, to a data identifier; and

the data identifier that identifies the input data based on the clock of the intermediate phase.

12. (Withdrawn) The clock data recovery circuit according to claim 11, wherein the first clock generating circuit includes

a frequency divider that divides a frequency of input data at a rise of the input data;

a phase comparator that detects a phase difference between a phase of the first clock and a phase of the input data of which frequency is divided by the frequency divider, and generates a phase difference signal to be used to eliminate the detected phase difference; and

a voltage control oscillator that generates the first clock by adjusting an oscillation frequency based on the phase difference signal, and outputs the first clock to both the phase combiner and the phase comparator, and

the second clock generating circuit includes

a frequency divider that divides a frequency of the input data at a fall of the input data;

a phase comparator that detects a phase difference between a phase of the second clock and a phase of the input data of which frequency is divided by the frequency divider, and generates a phase difference signal to be used to eliminate the detected phase difference; and

a voltage control oscillator that generates the second clock by adjusting an oscillation frequency based on the phase difference signal, and outputs the second clock to both the phase combiner and the phase comparator.